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## METHOD OF MANUFACTURING MOS TRANSISTOR

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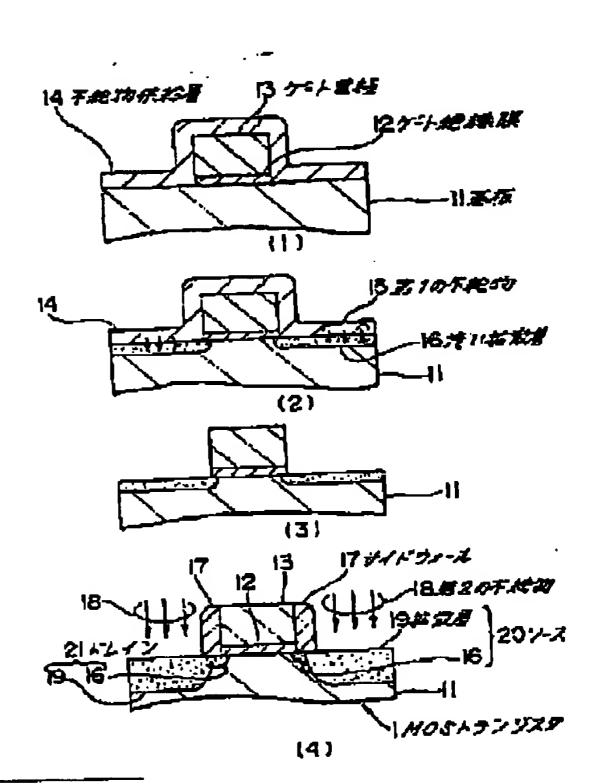
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## Abstract of JP8213605

PURPOSE: To provide a method of manufacturing a MOS transistor having a shallow diffused layer containing high

concentration impurities. CONSTITUTION: The method of manufacturing a MOS transistor is composed of four steps mentioned as follows, i.e., the first step of forming an impurity feeding layer 14 made of SiGe containing first impurities on a substrate 11 whereon a gate electrode 13 is formed in nonoxidative atmosphere through the intermediary of a gate insulating film 12, the second step of solid phase diffusing the impurities 15 from the impurity feeding layer 14 to the substrate 11 by heat treatment so as to form a source and drain shallow diffused layer 16 part, the third step of removing the impurity feeding layer 14 and the fourth step of, after forming a sidewall 17 on the sidewall of the gate insulating film 12 and the gate electrode 13, the second impurities 18 in the same conductivity type as that of the first impurities 15 are ionimplanted in the substrate 11 exposed from the sidewall 17 and the gate electrode 13 so as to form a source 20 and the diffused layer part 19 of a drain 21.



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